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<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p><i>(use as many sheets as necessary)</i></p> <p>Sheet 1 of 1</p>				Complete If Known		
				Application Number Filing Date First Named Inventor Art Unit Examiner Name Attorney Docket Number	Not assigned yet 10/767,069 On even date herewith S. SHUKURI Not assigned yet Not assigned yet 501.42645VX1	

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS

EXAMINER'S INVENTOR'S NON-PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), and other relevant information.
<i>JK</i>		"Can NROM, a 2 Bit, Trapping Storage NVM Cell, Give a Real Challenge to Floating Gate Cells?" Eitan et al., Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp.522-524
		"High Speed Program/Erase Sub 100 nm MONOS Memory Cell" Fujiwara et al., pp.75-77
		"A Novel Flash Memory Device with Split Gate Source Side Injection and ONO Charge Storage Stack (SPIN)" Chen et al., 1997 Symposium on VLSI Technology Digest of Technical Papers, pp. 63-64
<i>PR</i>		"Twin MONOS Cell with Dual Control Gates" Hayashi et al., Symposium on VLSI Technology Digest of Technical Papers, pp. 122-123

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PTO/SB/084 (10-01)

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		Application Number	10/767,069
		Filing Date	January 30, 2004
		First Named Inventor	S. SHUKURI
		Art Unit	Unknown
		Examiner Name	Unknown
		Attorney Docket Number	501.42645VX1

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BW		Takaaki NOZAKI, et al., A 1 Mbit EEPROM with MONOS Memory Cell for Semiconductor Disk Application, 1990 Symposium on VLSI Circuits, 1990 IEEE, (pp 101-102)

Examiner Signature		Date Considered	12/13/04
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